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EXAMINER	
LEUNG, CHRISTINA Y	

ART UNIT	PAPER NUMBER
2633	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,685	ARONSON ET AL.	
	Examiner	Art Unit	
	Christina Y. Leung	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-13,25 and 34-42* is/are allowed.

6)☒ Claim(s) *14-17,21,23,24 and 26-33* is/are rejected.

7)☒ Claim(s) *18-20 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-2-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 14-17, 21, 23, 24, and 26-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over King et al. (US 5,812,572 A) in view of Stephenson (US 2002/0027688 A1).

Regarding claim 14, King et al. disclose an optoelectronic device (Figure 1), comprising:

a laser transmitter 36; and

a controller (various circuit elements shown in Figure 1, including microcontroller 50);

wherein the controller comprises:

memory (the PROM, RAM, and EEPROM elements in microcontroller 50), including one or more memory arrays for storing information related to the optoelectronic device;

analog to digital conversion circuitry 52 for receiving a plurality of analog signals from the optoelectronic device, the analog signals corresponding to operating conditions of the optoelectronic device, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory (column 13, lines 49-67; column 14, lines 1-9); and

a memory interface 26 for allowing a host device to read from host specified locations within the memory in accordance with commands received from the host device (such as computer 90 in Figure 3; column 10, lines 10-18; column 16, lines 58-63).

Although King et al. also disclose a photodiode receiver 40, the receiver 40 receives a signal fed back from the transmitter; they do not specifically disclose a photodiode receiver together with the disclosed laser transmitter in a "transceiver" context (wherein the receiver would receive signals sent from an opposing communication device).

However, bidirectional optical communication using a transmitter and a receiver at both ends is well known in the art. Stephenson in particular teaches an optical communications system (Figures 2-4), including a laser transmitter 110 such as already disclosed by King et al., and further including a photodiode receiver 134 associated with that transmitter to provide a transceiver. It would have been obvious to a person of ordinary skill in the art to further include a receiver as taught by Stephenson in the system disclosed by King et al. in order to enable bidirectional communications between two locations.

Regarding claim 15, King et al. disclose generating a time value corresponding to cumulative operation time (referred to as "hours of operation" by King et al.) of the optoelectronic device, wherein the generated time value is readable via the memory interface (column 13, lines 64-67; column 14, lines 43-48; column 15, lines 42-50; Figure 12 shows that "hours of operation" is stored in memory). Similarly, regarding claim 16, King et al. disclose generating and storing in a register a time value corresponding to cumulative operation time of the optoelectronic device, wherein the register in which the time value is stored comprises one of the memory arrays of the memory (again, see Figure 12). Although King et al. do not explicitly show a "clock" element, it would be well understood in the art that King et al. inherently disclose some clock or time measurement element for providing the cumulative operation time value they explicitly disclose.

Regarding claim 17, King et al. disclose a power supply voltage sensor (shown as "power supply monitor" in Figure 1) coupled to the analog to digital conversion circuitry 52, the power supply voltage sensor generating a power level signal corresponding to a power supply voltage level of the optoelectronic device, wherein the analog to digital conversion circuitry is configured to convert the power level signal into a digital power level value and to store the digital power level value in a predefined power level location within the memory (column 16, lines 16-20);

wherein the predefined power level location is readable via the memory interface.

King et al. disclose that the interface 26 allows the host 90 to read "table entries" in the module (column 16, lines 58-66). King et al. further explicitly disclose that these table entries are stored as a memory map, whereby different table entries including power level information occupy different locations in memory (column 13, lines 64-67; column 14, lines 1-51).

Regarding claim 21, King et al. disclose a temperature sensor 56 coupled to the analog to digital conversion circuitry 52, the temperature sensor generating a temperature signal corresponding to a temperature of the optoelectronic transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory (column 13, lines 14-64);

wherein the predefined temperature location is readable via the memory interface.

King et al. disclose that the interface 26 allows the host 90 to read "table entries" in the module (column 16, lines 58-66). King et al. further explicitly disclose that these table entries are stored

as a memory map, whereby different table entries including temperature values occupy different locations in memory (column 13, lines 64-67; column 14, lines 1-51).

Regarding claim 23, King et al. disclose fault handling logic (i.e., the logic circuits in microcontroller 50), coupled to the optoelectronic device for receiving at least one fault signal from the optoelectronic device, coupled to the memory (i.e., the EEPROM) to receive at least one flag value stored in the memory, and coupled to a host interface (serial port 26) to transmit a computed fault signal (referred to as an "alarm" by King et al.), the fault handling logic including computational logic for logically combining the at least one fault signal received from the optoelectronic transceiver and the at least one flag value received from the memory to generate the computed fault signal (column 14, lines 60-64; column 16, lines 8-38).

Examiner notes that although other claims in the present application recite "flag values" in greater detail (such as claim 1, which specifically recites the flag values are values generated by comparing digital values with limit values, etc), claim 23 and claim 14 on which the claim depends do not recite such further details regarding the at least one flag value. King et al. discloses "flag values" stored in memory such as predetermined thresholds/limits and "end-of-life" criteria; an extraordinary input from the optoelectronic device received by the microcontroller (i.e., a "fault signal") is compared to these flag values, and an alarm (i.e., a "computed fault signal" is generated (column 14, lines 60-64; column 16, lines 8-38).

Regarding claim 24, King et al. disclose that the plurality of analog signals includes laser bias current and laser output power (Figure 1, for example, shows inputs to the analog-to-digital converter 52 from "average bias monitor" and "power supply monitor").

Regarding claims 26 and 29, King et al. disclose an optoelectronic device (Figure 1), comprising:

a laser transmitter 36;

a controller (various circuit elements shown in Figure 1, including microcontroller 50);

wherein the controller comprises:

memory (the PROM, RAM, and EEPROM elements in microcontroller 50), including one or more memory arrays for storing information related to the optoelectronic device;

analog to digital conversion circuitry 52 configured to receive at least one or a plurality of analog signals, the analog signals corresponding to operating conditions of the optoelectronic device, converting at least one of the received analog signals into at least one digital value, and storing the at least one digital value in at least one predefined location within the memory (column 13, lines 49-67; column 14, lines 1-9); and

a memory interface 26 for allowing a host device to read from host specified locations within the memory in accordance with commands received from a host device (such as computer 90 in Figure 3; column 10, lines 10-18; column 16, lines 58-63).

.As similarly discussed above with regard to claim 14, although King et al. also disclose a photodiode receiver 40, the receiver 40 receives a signal fed back from the transmitter; they do not specifically disclose a photodiode receiver together with the disclosed laser transmitter in a "transceiver" context (wherein the receiver would receive signals sent from an opposing communication device).

Regarding claims 27 and 30 (which depend on claims 26 and 29 respectively), King et al. disclose a temperature sensor 56 coupled to the analog to digital conversion circuitry 52, the

temperature sensor generating a temperature signal corresponding to a temperature of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in the at least one predefined location within the memory (column 13, lines 14-64);

wherein the at least one predefined location storing the digital temperature value is readable via the memory interface.

King et al. disclose that the interface 26 allows the host 90 to read "table entries" in the module (column 16, lines 58-66). King et al. further explicitly disclose that these table entries are stored as a memory map, whereby different table entries including temperature values occupy different locations in memory (column 13, lines 64-67; column 14, lines 1-51).

Regarding claims 28 and 32 (which depend on claims 26 and 29 respectively), King et al. disclose that the analog to digital conversion circuitry is configured to receive a voltage signal from a source external to the controller (such as from "power supply monitor" shown in Figure 1), wherein the analog to digital conversion circuitry is configured to convert the voltage signal into a digital voltage value and to store the digital voltage value in the at least one predefined location within the memory (column 16, lines 16-20);

wherein the at least one predefined location storing the digital voltage value is readable via the memory interface.

King et al. disclose that the interface 26 allows the host 90 to read "table entries" in the module (column 16, lines 58-66). King et al. further explicitly disclose that these table entries are stored as a memory map, whereby different table entries including power level information occupy different locations in memory (column 13, lines 64-67; column 14, lines 1-51).

Regarding claim 31, King et al. disclose control circuitry (modulation current adjust 24 and bias control circuitry 30, for example), responsive to the digital temperature value for controlling operation of the optoelectronic device (column 16, lines 26-31; column 18, lines 4-14).

Regarding claim 33, King et al. disclose control circuitry (modulation current adjust 24 and bias control circuitry 30, for example), responsive to the at least one digital value for controlling operation of the optoelectronic device (column 16, lines 26-31; column 18, lines 4-14).

Allowable Subject Matter

3. Claims 1-13, 25, and 34-42 are allowed. Claims 18-20 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for the indication of allowable subject matter were given in the previous Office Action.

Response to Arguments

4. Applicants' arguments filed 23 November 2004 with respect to claims 14-17, 21, 23, 24, and 26-33 have been fully considered but they are not persuasive.

5. Examiner respectfully disagrees with Applicants assertion on pages 14-16 of their response that King et al. does not disclose "...a memory interface for allowing a host to read from host specified locations within the memory in accordance with commands received from a host device."

First, King et al. disclose a host device (computer 90) that is connected to a laser diode transmitter module 80 as shown in Figure 3 via a communication interface 89, which connects to the interface element 26 shown in Figure 1 (column 10, lines 10-14; column 16, lines 58-62) .

Second, King et al. disclose that the microcontroller 50 (which contains the memory arrays in the module) receives commands from host device 90 regarding reading the memory:

"Serial interface 26 provides valuable interface for purposes of allowing a host computer or communication system to interrogate or communicate with microcontroller 50, thereby enabling monitoring and changing operation parameters without interruption of service. In such embodiments, A/D channels of the module may be monitored, D/A channels may be loaded, table entries may be monitored and/or changed, and statistical information may be gathered..." (column 16, lines 58-66)

Figure 14 also shows in the functioning of the microcontroller 50, which includes steps 228 and 230 ("Process host request (read memory, write memory...)").

Third, King et al. disclose that the host device 90 is able to read from host-specified locations in memory. Specifically, King et al. disclose that the interface 26 allows the host 90 to read "table entries" in the module (see column 16, lines 58-66 quoted above). King et al. further explicitly disclose that these table entries are stored as a memory map, whereby different table entries occupy different locations in memory:

"Fig. 12 illustrates a table of discrete values for an exemplary memory map in microcontroller 50 that is utilized in preferred embodiments of the present invention. Each entry in the table indicates the values to be used for the corresponding temperature. Each line entry in the table represents an incremental change in temperature." (column 13, lines 64-67; column 14, lines 1-3)

Further regarding these tables, King et al. also refer to "storing the associated modulation current in a first location of memory associated with the particular value of the operating condition" (column 20, lines 62-63).

Examiner notes that the claim only recites "a memory interface *for allowing* a host to read from host specified locations within the memory in accordance with commands received from a host device." Clearly King et al. disclose an interface between a host and the memory in the module, since the host reads the memory. Examiner respectfully submits that King et al. further disclose that the host sends commands to (i.e., "interrogates" as previously quoted) the module in order to select what type of information it would like to read. Examiner respectfully submits that King et al. further disclose that the serial interface 26/89 (the interface that is shown as element 26 in Figure 1 and element 89 in Figure 3) "allows" host 90 to read certain locations in the module memory (such as corresponding to table entries) in accordance with commands that the host sends.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christina Y. Leung whose telephone number is 571-272-3023. The examiner can normally be reached on Monday to Friday, 6:30 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on 571-272-3022. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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